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EFM32G Hardware Design Considerations

Application Note

0 1 2 3 4

Introduction

This application note is intended for system designers who require an overview of the hardware design considerations for the EFM32G. Topics that are handled specifically are how to provide a robust supply power to the chip, connection to the debug interface and using external clock sources like crystals and ceramic resonators.

The scope is to provide an introduction to potential design challenges, and not to give an exhaustive description of how to design different applications with the EFM32G.

1 Power Supply

1.1 Introduction

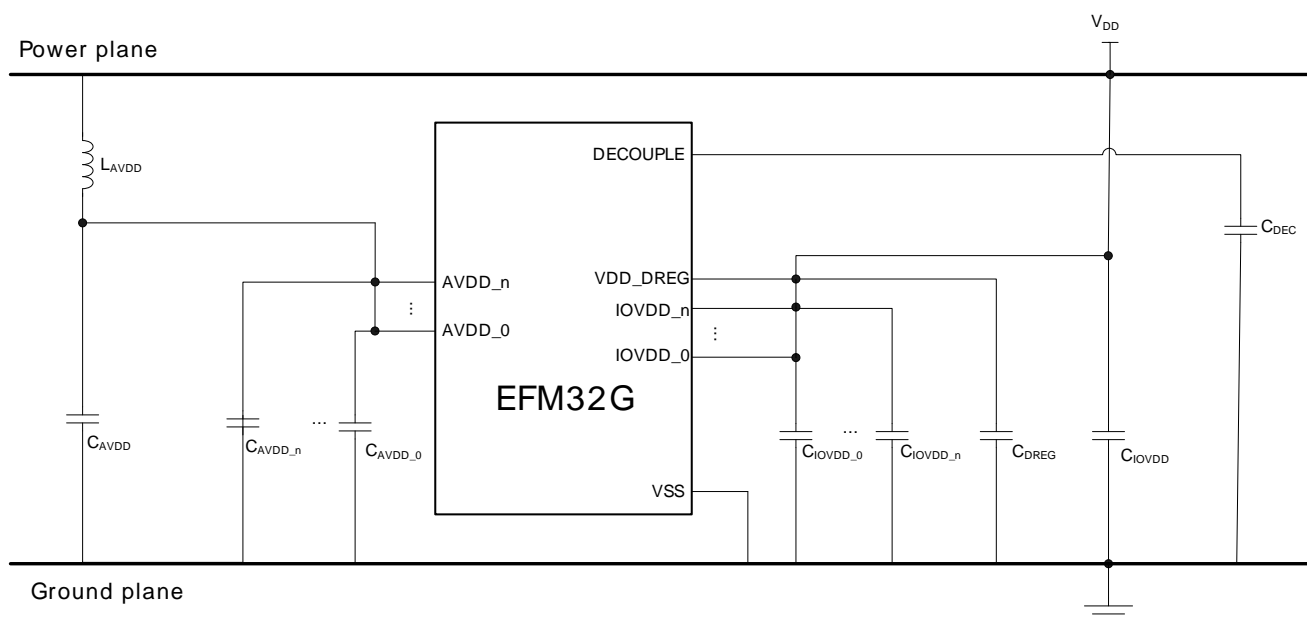
Even though the EFM32G supports a wide voltage range and has an exceptionally small average supply current consumption, proper decoupling is crucial. As for all digital circuits, the current is drawn in short pulses occurring on the clock edges. Particularly when several I/O lines are switching simultaneously, the current pulses on the power supply lines can be in the order of several hundred mA. If the I/O lines are not loaded the pulse width may be only a few ns. Therefore, even if the average current consumption of the EFM32G is very small, the current drawn during short pulses can be considerable.

Such kind of current spikes cannot be properly delivered over long power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, which could degrade the performance of the EFM32G, the solution is to use decoupling capacitors which can act as supplementing current sources during these short transients.

1.2 Power Supply Decoupling

All power pins must be connected to external decoupling capacitors as indicated in Figure 1.1 (p. 2) .

Figure 1.1. Power supply



The number of analog power pins (AVDD_n), I/O power pins (IOVDD_n) and ground pins (VSS) depend on the device package. Please refer to the EFM32G datasheet for package and pinout information. In order to protect the built-in analog modules of the EFM32G devices from digital switching noise, the analog power must be decoupled separately. This is particularly important to ensure high accuracy for the built-in ADC.

All external decoupling capacitors should have a temperature range reflecting the environment in which the EFM32G should be used. Ceramic capacitors with X5R material with a change in capacitance of ±15% over the temperature range -55°C - +85°C would be a good choice covering the entire operating temperature range of the EFM32G with a reasonable accuracy.

1.2.1 Decoupling of Analog Power

Close to each of the analog power pins, a decoupling capacitor $C_{AVDD_n} \sim 10$ nF should be placed, ref. Figure 1.1 (p. 2). Additionally a common decoupling capacitor $C_{AVDD} \sim 10$ μ F should be connected between the analog power pins and ground.

An inductor in series between the analog pins and V_{DD} would further improve the switching noise of the analog power. The inductor gives a relatively high impedance path between the power plane and the analog power pins during current pulses, effectively reducing the noise in the power plane. Evidently, the series resistance of the inductor must be so small that it does not give a significant DC voltage drop. (An EMI/RFI suppressor similar to BLM21B102S could be a good choice for L_{AVDD})

1.2.2 Decoupling of I/O Power

Close to each of the I/O power pins, a decoupling capacitor $C_{IOVDD_n} \sim 100$ nF should be placed, ref. Figure 1.1 (p. 2). The VDD_DREG pin, which supplies the EFM32G internal digital regulator, can be decoupled with a similarly sized capacitor, C_{DREG} . Additionally a common decoupling capacitor $C_{IOVDD} \sim 10$ μ F should be connected between the power plane and ground.

1.2.3 Decouple Pin

This pin is to provide external decoupling to the internal regulated supply power. This capacitor, C_{DEC} , (ref. Figure 1.1 (p. 2)) should be in the order of 1 μ F to filter transients from this power domain.

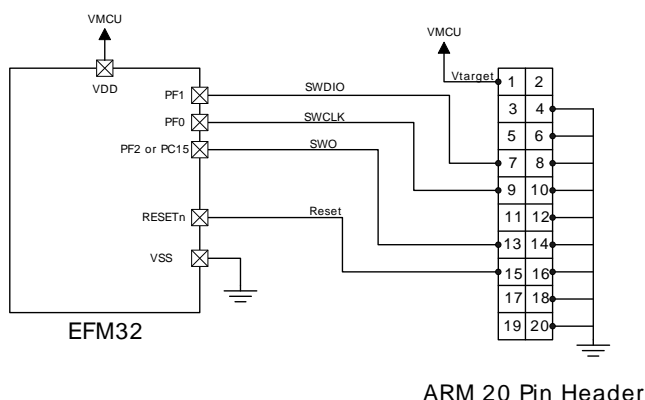
2 Debug Interface and External Reset Pin

2.1 Debug Interface

The debug interface basically consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO (serial wire output). The SWO line is for example used for instrumentation trace and program counter sampling, and is not needed for programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and it is therefore recommended to include this line in a design.

The connection to an ARM 20 pin debug connector is shown in Figure 2.1 (p. 4). Pins with no connection should be left unconnected.

Figure 2.1. Connecting the EFM32 to an ARM 20 pin debug header



2.2 External Reset Pin (RESETn)

Forcing the RESETn pin low generates a reset of the EFM32G. The RESETn pin includes an internal pull-up resistor and can therefore be left unconnected if no external reset source is required. Also connected to the RESETn line is a low-pass filter which prevents noise glitches from resetting the EFM32G. The characteristics of the pullup and input filter is identical to the corresponding characteristic of a GPIO pin, which is found in the device datasheet.

3 External Clock Sources

3.1 Introduction

The EFM32G supports different external clock sources to generate the low and high frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how the external clock sources should be connected and gives a brief introduction to some special considerations with regards to crystals and ceramic resonators.

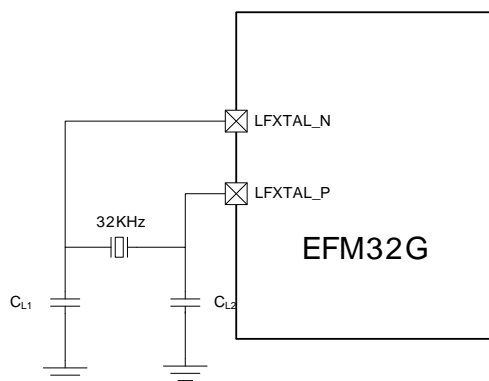
3.2 Low Frequency Clock Sources

The external low frequency clock can be generated from a crystal/ceramic resonator or from an external clock source.

3.2.1 Low Frequency Crystals and Ceramic Resonators

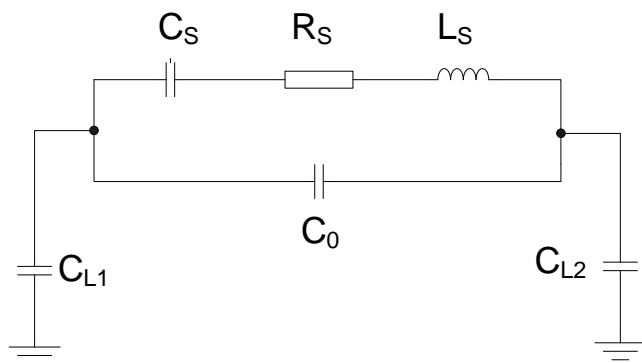
The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.1 (p. 5). The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32G.

Figure 3.1. Low Frequency Crystal



The crystals/ceramic resonators oscillate mechanically and have an electrical equivalent circuit as shown in Figure 3.2 (p. 5). In the electrical circuit C_S represents the motional capacitance, L_S the motional inductance, R_S the mechanical losses during oscillation and C₀ the parasitic capacitance of the package and pins. C_{L1} and C_{L2} represent the load capacitance. This circuit is valid for both crystals and ceramic resonators. For information of the component values in the equivalent circuit, please refer to the crystal/ceramic resonator vendor's datasheet.

Figure 3.2. Equivalent Circuit of a Crystal/Ceramic Resonator



The series resonant frequency of the crystal/ceramic resonator can be calculated in accordance with Equation 3.1 (p. 6) .

Crystal/Ceramic Resonator Series Resonant Frequency

$$f=1/(2 \pi (L_S C_S)^{1/2}) \quad (3.1)$$

The Q-factor of the crystal/ceramic resonator, which is a measure of frequency tolerance is given by Equation 3.2 (p. 6)

Crystal/Ceramic Resonator Q-Factor

$$Q=X_{L_S}/R_S= 1/ (X_{C_S} \times R_S) \quad (3.2)$$

where X_{L_S} and X_{C_S} are the reactance of L_S and C_S , respectively, at the operating frequency of the crystal/ceramic resonator.

As seen in Figure 3.2 (p. 5) two capacitors C_{L1} and C_{L2} are the load of the crystal. They include the external load capacitor of the crystal and the parasitic capacitance of each pin. The effective load capacitance, C_L , as seen from the LFXTAL_N and LFXTAL_P pins is the series combination of C_{L1} and C_{L2} .

Effective Load Capacitance

$$C_L= (C_{L1} \times C_{L2})/ (C_{L1} + C_{L2}) \quad (3.3)$$

Right choice of C_L is important for proper operating frequency. For more information please refer to the crystal vendor's datasheets. It is recommended to use a crystal with C_L as specified in the EFM32G datasheet.

The Equivalent Series Resistance (ESR) value is the electrical representation of the mechanical losses of the crystal/ceramic resonator during oscillation. ESR can be calculated with the formula.

Equivalent Series Resistance

$$ESR=R_S(1+C_0/C_L)^2 \quad (3.4)$$

The LF crystal oscillator circuit of the EFM32G has a limitation and can not guarantee startup of crystals and ceramic resonators with ESR larger than a certain limit. Please refer to EFM32G datasheet for further details. The smaller the ESR, compared to this maximum value, the better margin for startup of the crystal. Additionally, if current consumption is a main concern, a small ESR value also gives smaller current consumption during oscillation.

Another important parameter with regard to the crystal/ceramic resonator is startup time, which is typically in the order of some hundred milliseconds for 32.768 kHz. The startup time depends on several factors. First, evidently the oscillator frequency influences the startup time. A crystal in the kHz range would have a considerably longer startup timer than a crystal in the MHz range. Second, high Q-factor crystals will normally start slower than crystals with higher frequency tolerance. Typically, crystals have higher Q-factor than ceramic resonators. Crystals would therefore be expected to have a longer startup time than ceramic resonators. Crystals with small load capacitance would typically start faster than crystals requiring high load capacitance. Finally, crystals with low ESR could be expected to have a shorter startup time than crystals with high ESR.

In some applications a high frequency tolerance of for example 1% can be accepted, and an inexpensive ceramic resonator with fast startup time could be applied. In other cases, however, a high accuracy clock is required (e.g. 0.001%). In such applications a fast startup time may have to be traded in order to obtain the required accuracy.

In general one would like the circuit to be operational as fast as possible and a fast startup time is therefore favourable. During startup the current consumption is higher than after oscillation has

stabilized. A fast startup time therefore reduces the period of which the current consumption of the oscillator is high. This is particularly important in applications where the oscillator is frequently switched on and off.

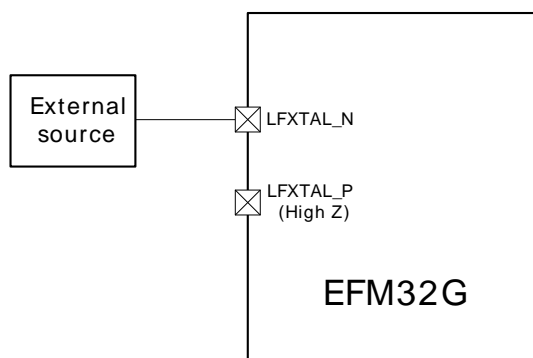
Additionally it is of high importance to keep the lines between the crystal and eventual external capacitors and the EFM32G as short as possible. Very small currents are running in the crystal oscillator and long lines make it more sensitive to EMC, ESD and crosstalk. Long lines also add parasitic capacitance and some series resistance to the oscillator. It is also recommended to guard the crystal traces with ground traces and keep other clock lines and signal lines that are switching frequently as far away from the crystal connections as possible.

3.2.2 Low Frequency External Clocks

The EFM32G can also be clocked by a LF external clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency of 32.768 kHz. The external clock source must be connected as indicated in Figure 3.3 (p. 7).

When a square wave source is used the LFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%, as specified in the EFM32G datasheet. When a sine source is used, the amplitude must be in accordance with the EFM32G datasheet. The sine signal is buffered through the LFXO buffer, whose input is AC-coupled.

Figure 3.3. Low Frequency External Clock



3.3 High Frequency Clock Sources

The external high frequency clock can be generated from a crystal/ceramic resonator or from an external square or sine wave source.

3.3.1 High Frequency Crystals and Ceramic Resonators

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 3.4 (p. 8). The crystal is to be connected across the HFXTAL_N and HFXTAL_P pins.

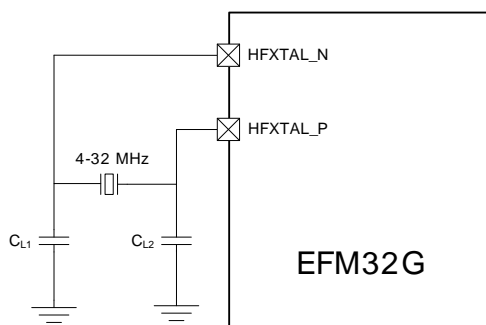
The electrical equivalent circuit of the HF crystal/ceramic resonators is equal to the one for LF crystals/ceramic resonators in Figure 3.2 (p. 5). The component values of the equivalent circuit will of course reflect the frequency, ESR and Q-factor of the HF crystal/ceramic resonator. The effective load capacitance, C_L , as seen from the HFXTAL_N and HFXTAL_P pins is the series combination of C_{L1} and C_{L2} , ref. Equation 3.3 (p. 6).

Right choice of C_L is important for proper operating frequency. For more information please refer to the crystal vendors' datasheets. It is recommended to use a fundamental mode crystal with C_L of in the range as specified in the EFM32G datasheet.

The ESR, as given in Equation 3.4 (p. 6), will typically decrease with increasing oscillation frequency. The EFM32G supports crystals with ESR as specified in the EFM32G datasheet. As for the LF crystal/ceramic resonator a small ESR value is preferable as it improves startup margin and reduces current consumption.

As for the LF domain, it is important to keep the lines between the crystal, external capacitors and the EFM32G as short as possible. Small currents are running in the crystal oscillator and long lines make it more sensitive to EMC, ESD and crosstalk. Long lines also add parasitic capacitance to the oscillator. Additionally, long lines will introduce series resistance which could reduce the startup margin of the crystal. Note that HF crystals/ceramic resonators have ESR of a few tens of Ohm's as compared to the LF crystals/ceramic oscillators which have ESR values normally measured in kOhm. Therefore a few Ohm of series resistance has more influence on the startup margin in the MHz range as compared to the kHz range. It is also recommended to guard the crystal traces with ground traces and keep other clock lines and signal lines that are switching frequently as far away from the crystal connections as possible.

Figure 3.4. High Frequency Crystal Oscillator

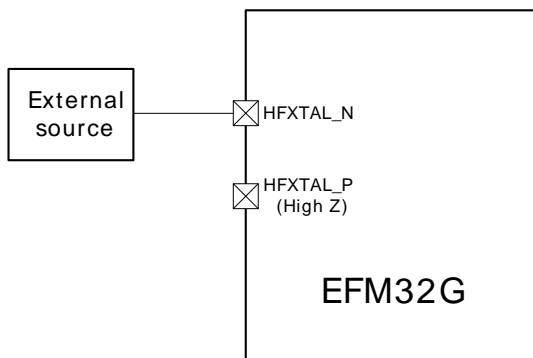


3.3.2 High Frequency External Clocks

The EFM32G can also be clocked by an external HF clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock signal can either be square wave or a sine signal with a frequency in accordance with the EFM32G datasheet. The external clock source must be connected as indicated in Figure 3.5 (p. 8).

When a square wave source is used the HFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%. Please refer to the EFM32G datasheet for further details. When a sine source is used, the sine amplitude must be in accordance with what is specified in the EFM32G datasheet. The sine signal is buffered through the HFXO buffer, whose input is AC-coupled.

Figure 3.5. External High Frequency Clock



4 Revision History

4.1 Revision 1.10

Added debug interface section, May 6th, 2010

4.2 Revision 1.00

Initial revision, October 21st, 2009

A Disclaimer and Trademarks

A.1 Disclaimer

Energy Micro AS intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the EFM32G microcontrollers. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and “Typical” parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only, and Energy Micro accepts no liability for inclusion and/or use in such equipment or applications resulting in personal injury, death or severe property or environmental damage. Energy Micro reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Energy Micro shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits.

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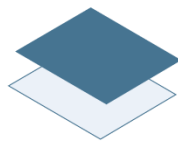
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